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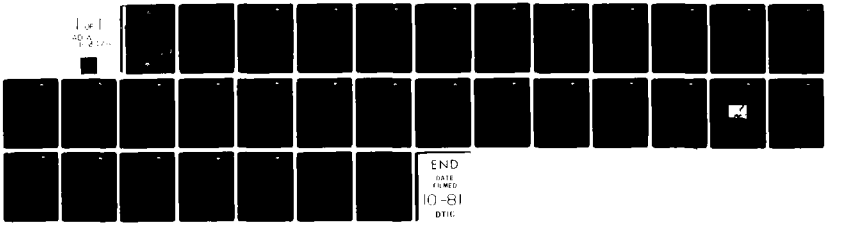

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MONOLITHIC GaAs OSCILLATOR DEVELOPMENT

FINAL REPORT FOR THE PERIOD
July 15, 1979 through October 14, 1980

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Prepared for

Office of Naval Research
800 North Quincy St.
Arlington, VA. 22217

D. Richard Decker
Principal Investigator

JULY 1981

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Design considerations and test results for a GaAs monolithic varactor tuned X-band oscillator are presented. Analysis of the test results and recommendations for further work are included.

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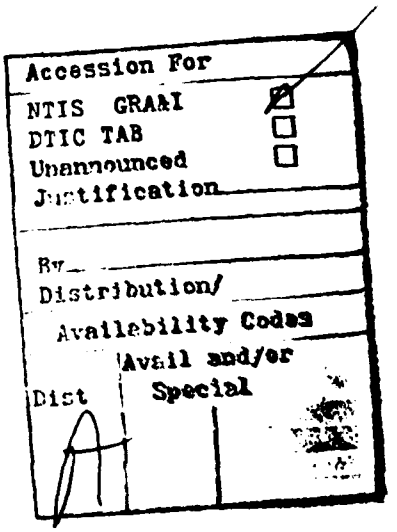
FOREWORD

This is the final report for ONR Contract No. N00014-79-C-0726 describing work performed between 15 July 1979 and 14 Oct 1980. Later phases of this program are continuing as part of ONR Contract No. N00014-78-C-0624. The goal of this program is to develop an 8 GHz monolithic GaAs, voltage-controlled, stabilized oscillator suitable for monolithic integration with an 8 GHz satellite communications-band receiver front-end. The work described herein was carried out at Rockwell International Microelectronics Research and Development Center, P.O. Box 1085, Thousand Oaks, California.

The program manager and principal investigator was Dr. D. R. Ch'en. Other members of staff who have contributed to this program are: Drs. D. R. Decker, A. K. Gupta, and W. C. Petersen. Mr. M. N. Yoder of the Office of Naval Research was the technical monitor of this program.



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1.0 INTRODUCTION

This final report describes the work performed under ONR Contract No. N00014-79-C-0726 between 15 July 1979 and 14 Oct 1980. The goal of this program was to develop an 8 GHz monolithic voltage controlled stabilized oscillator on gallium arsenide (GaAs) suitable for monolithic integration with an 8 GHz satellite communications band receiver front-end. The monolithic microwave integrated circuit (MMIC) design is based on microstrip circuitry fabricated on a semi-insulating GaAs substrate with resistivity as high as 10^9 Ω-cm. Active devices (FETs and varactors), bias networks, and microwave circuitry are fabricated on a single GaAs chip. Ion implantation doping technology facilitates control of doping densities for optimization of FET and varactor active devices and also permits fabrication of highly planar circuits to achieve superior yields.

The monolithic stabilized oscillator fabricated under this program contains a varactor tuned common-drain oscillator, a common-source buffer amplifier for gain and load isolation, and an active output coupler which provides a sample output to facilitate phase locked operation.

This report is organized as follows. Section 2.0 describes the program objectives, the design approach, and a detailed circuit design. A discussion of the fabrication technology is contained in Section 3.0, followed by test results and further analysis in Section 4.0. Finally, Section 5.0 provides a summary and recommendations for work under Phase 2 of this program.

2.0 OSCILLATOR DESIGN

The objective of the monolithic GaAs stabilized oscillator technology program, the design approach used to meet these objectives, and a detailed circuit design based on this approach are described below.

2.1 Objectives and Design Approach

The objectives of this program are to:

1. design and fabricate a monolithically integrated oscillator on GaAs for operation in the 8 GHz satellite communication band,
2. characterize the oscillator and assess its compatibility with the other components of a monolithically integrated microwave receiver or frequency down-converter, and
3. assess the suitability of various frequency stabilization techniques for use in monolithically integrated microwave oscillators.

One of the most important considerations in the selection of a design approach for monolithic integrated circuits is the compactness of the final circuit. A small circuit is essential for high yield, mechanical strength, potential low cost, and the potential of further integration into larger subsystems. Therefore, microstrip circuitry was selected as the transmission medium over co-planar transmission lines, slot lines, and other space consuming modes of transmission. Microstrip also simplifies the testing and packaging since a good ground plane is available on the chip back surface, which also provides a convenient heat sink (not of primary importance in this application due to the low power dissipation of the monolithic oscillator). The thickness of the GaAs substrate is then selected as a compromise between conflicting requirements. A thick substrate is desired to obtain a high maximum transmission line impedance, low loss, low parasitic capacitance to the ground plane, and mechanical strength. A thin substrate provides low

coupling between adjacent transmission lines for small size, and an improved heat sinking capability. The need for low impedance transmission lines is substantially reduced by the availability of lumped metal-insulator-metal capacitors. A substrate thickness of 250 microns was selected for this application, which provides a maximum transmission line impedance of approximately 100 ohms (for a width of 15 microns) and allows implementation of the oscillator circuit on a 2 mm × 2 mm chip of GaAs.

Selection of an oscillator circuit design approach and the design of on-chip peripheral circuits is also governed by the need for a compact layout. Whenever possible, large passive structures are replaced by either active devices or equivalent but smaller passive configurations. Based on these considerations a varactor-tuned common-drain FET oscillator with a one-stage, common-source, buffer amplifier has been selected. Due to the small physical size of the oscillator and the low Q of the elements available on-chip, an off-chip stabilization technique is required. Toward this end, the oscillator is voltage tunable via varactor diodes in the resonator circuit, and an isolated sample of the RF output signal is provided. An active device is used for the sampling function to conserve space. The oscillator chip designed along these lines can then be tested in a variety of configurations. For example, several phase-locked oscillator configurations can be created by the addition of an external mixer(s), a loop amplifier, a filter, and possibly a frequency prescaler. Provision is also made for the direct connection of a high Q external passive resonator.

2.2 Circuit Design

Oscillator Stage

The basic common-drain oscillator circuit is shown in Fig. 2.1. Further connections will be added to provide varactor tuning, a buffer amplifier, and a sampled RF output; however, as much of the inherent simplicity as possible is retained throughout the design process. The oscillator starting conditions can be derived from the simplified small signal equivalent circuit

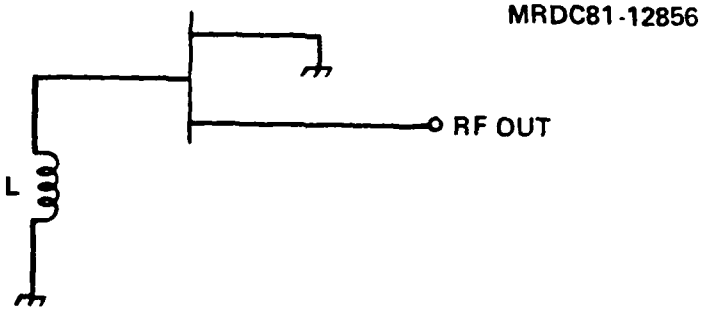

Fig. 2.1 Common drain FET oscillator.

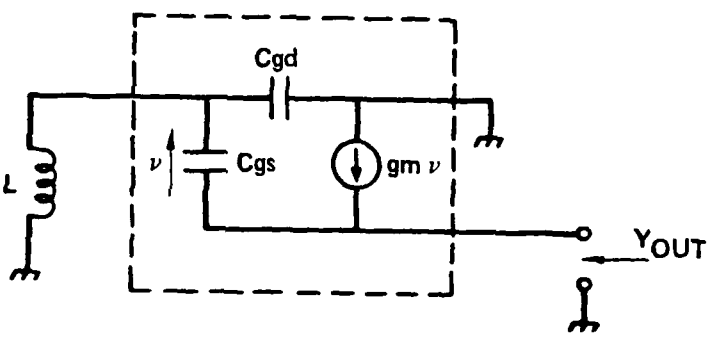

Fig. 2.2 Simplified model of the common drain oscillator.

shown in Fig. 2.2, which contains only the relevant FET parasitic elements. A more detailed model of the oscillator circuit, which includes all known parasitic elements, was used in an interactive manner to obtain the final oscillator layout described later in this section.

Straightforward analysis of Fig. 2.2 leads to the following expression for the oscillator output admittance:

$$Y_{out} = (g\hat{m} + j\omega C_{gs})\, K$$

where

$$K = \frac{\omega^2 C_{gd} L - 1}{\omega^2 L\,(C_{gs} + C_{gd}) - 1} \quad .$$

Note that the real part of Y_{out} is negative for $K < 0$ and that under these conditions Y_{out} always contains an inductive parasitic susceptance component. Therefore, the load presented to the oscillator must be capacitive at the frequency of oscillation. The parasitic drain to source capacitance, C_{ds}, (not shown in Fig. 2.2) will be part of this required load capacitance. Further analysis yields the following frequency bounds on the negative admittance region of Y_{out}:

$$\frac{1}{\sqrt{(C_{gs} + C_{gd})L}} < \omega < \frac{1}{\sqrt{C_{gd} L}} \quad .$$

As C_{gd} approaches zero, the upper frequency limit becomes infinite for this simplified model. In practice, parasitic resistances will limit the upper frequency of operation, but C_{gd} must be kept as small as possible to avoid unnecessary limitations on oscillator performance. For a typical FET with a 300 micron wide by one micron long gate operated at 20 milliamps, C_{gs} is approximately 0.2 pF and C_{gd} is approximately 0.015 pF. Calculations of

the band of negative resistance as a function of gate inductance are summarized in Table 2.1 for these values of capacitance.

Table 2.1

L(nH)	Frequency Band (GHz)	
1.0	10.9	41.1
1.5	8.9	33.6
2.0	7.7	29.1
2.5	6.9	26.0
3.0	6.3	23.7

As expected, when the lumped inductor is replaced by a 100 ohm shorted stub the bandwidth of negative conductance shrinks; however, it is still acceptable as shown in Table 2.2. The same values of C_{gs} and C_{gd} were used in Tables 2.1 and 2.2. Higher frequency bands of negative conductance are also available when a shunt stub is used due to its periodic susceptance as a function of frequency, but they are not considered for this application.

Table 2.2

Delay Length (ps)	Frequency Band (GHz)	
5.0	7.5	13.8
6.0	6.7	11.6
7.0	6.1	10.0
8.0	5.6	8.8

For a load impedance of $Y_L = G_L + j\omega C_L$, oscillations start at the frequency where the load capacitance resonates with the output inductance of the oscillator, provided that G_L is less than the negative of the output conductance. Therefore, at the starting frequency:

$$C_L = -KC_{gs}$$

and

$$G_L < -gm\ K \quad .$$

The latter condition further reduces the available oscillator bandwidth once a load conductance is selected. Oscillator tuning can be achieved in three ways. Variation of the load capacitor, variation of C_{gs}, variation of the gate tuning inductor, or any combination of these can be used to control the frequency of oscillation. Tuning of the load capacitance is undesirable due to the large RF signal at this point which tends to reduce the available varactor tuning range. One of the major reasons for including the buffer amplifier is to reduce load pull effects on the oscillator. Tuning of either the gate inductor, L, or the gate to source capacitance, C_{gs}, are acceptable, and provision for both is incorporated in the final design.

A variable inductance is obtained from the parallel connection of a shorted stub and a varactor diode operating below resonance. Tuning the varactor from the smallest possible capacitance to parallel resonance provides an inductance which varies from the inductance of the stub alone up to infinite inductance at resonance. C_{gs} is adjusted by varying the gate to source voltage of the oscillator FET.

Buffer Amplifier and Sample Output

The buffer amplifier and its associated source follower, which provides the sample output, are designed to meet the following requirements:

1. present an optimum load, Y_L, to the common drain oscillator,
2. provide power gain with load isolation,
3. maintain a good output match, and
4. supply an isolated sample output for phase locking.

In addition, the final circuit design must have all required biasing networks and bypass circuitry to reduce sensitivity to assembly variations during testing. A circuit which meets these goals is shown in Fig. 2.3, which is a schematic of the entire monolithically integrated voltage controlled oscillator. The varactor diode is implemented as two varactor diodes in series to reduce the effect of the RF signal level on varactor tuning range. Two shunt resistors are provided to equalize the bias voltage drop across the varactors which may not have identical leakage currents. Each resistor is large enough to avoid degradation of the varactor Q. To further reduce the RF signal level, only part of the inductive stub is bypassed by the varactors. The 100 ohm source resistor provides an oscillator load and in addition allows DC bias of the oscillator FET. The RF signal is coupled to a common-source buffer amplifier output stage, which is tuned to an output impedance of 50 ohms by the shunt stub and a series output capacitor. The shunt stub provides a convenient drain bias line while the series tuning capacitor eliminates the DC bias voltage from the RF output port. A small source follower samples the signal and provides a low-level sample output signal matched to approximately 50 ohms. No DC blocking is provided on this output in order to allow more flexible biasing of the amplifier stage. A photograph of the monolithic chip implementing this circuit is shown in Fig. 3.1.

A detailed computer analysis of several aspects of the circuit shown in Figs. 2.3 and 3.1 was used to verify the design prior to mask generation and circuit fabrication. First, a large-signal analysis program (a modified version of SPICE) was used to model the oscillator portion of the circuit to insure that oscillations would start and grow as predicted by the small signal model. The time domain output predicted by SPICE is shown in Fig. 2.4 for a high frequency tuning of the varactors (considered the tuning most likely to cause problems). The program was not run to a steady state condition (as evidenced by the non-zero DC component of the output even though a blocking capacitor is included in the model) due to the large amount of computer time required. However, it is clear that the signal is growing rather than decaying, and that the oscillation frequency is approximately 9.5 GHz for this

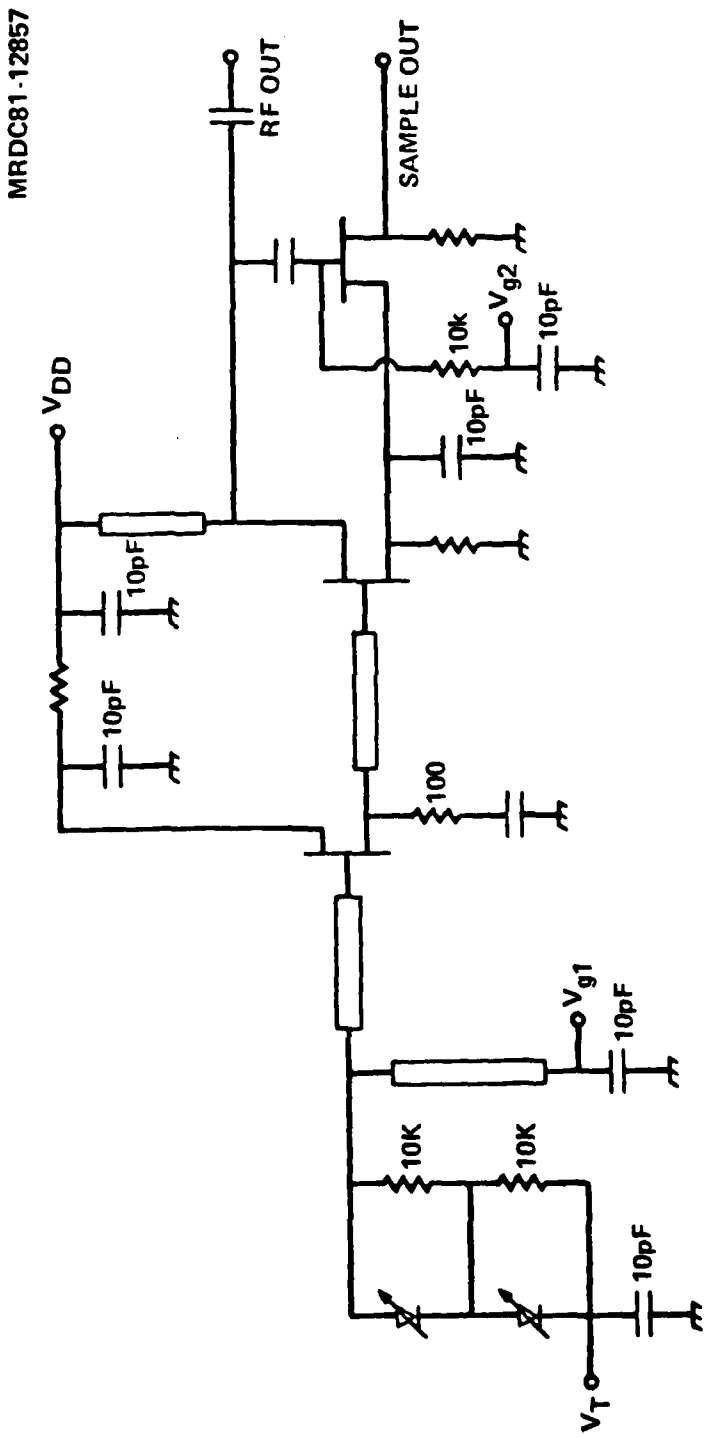

Fig. 2.3 Voltage controlled oscillator schematic.

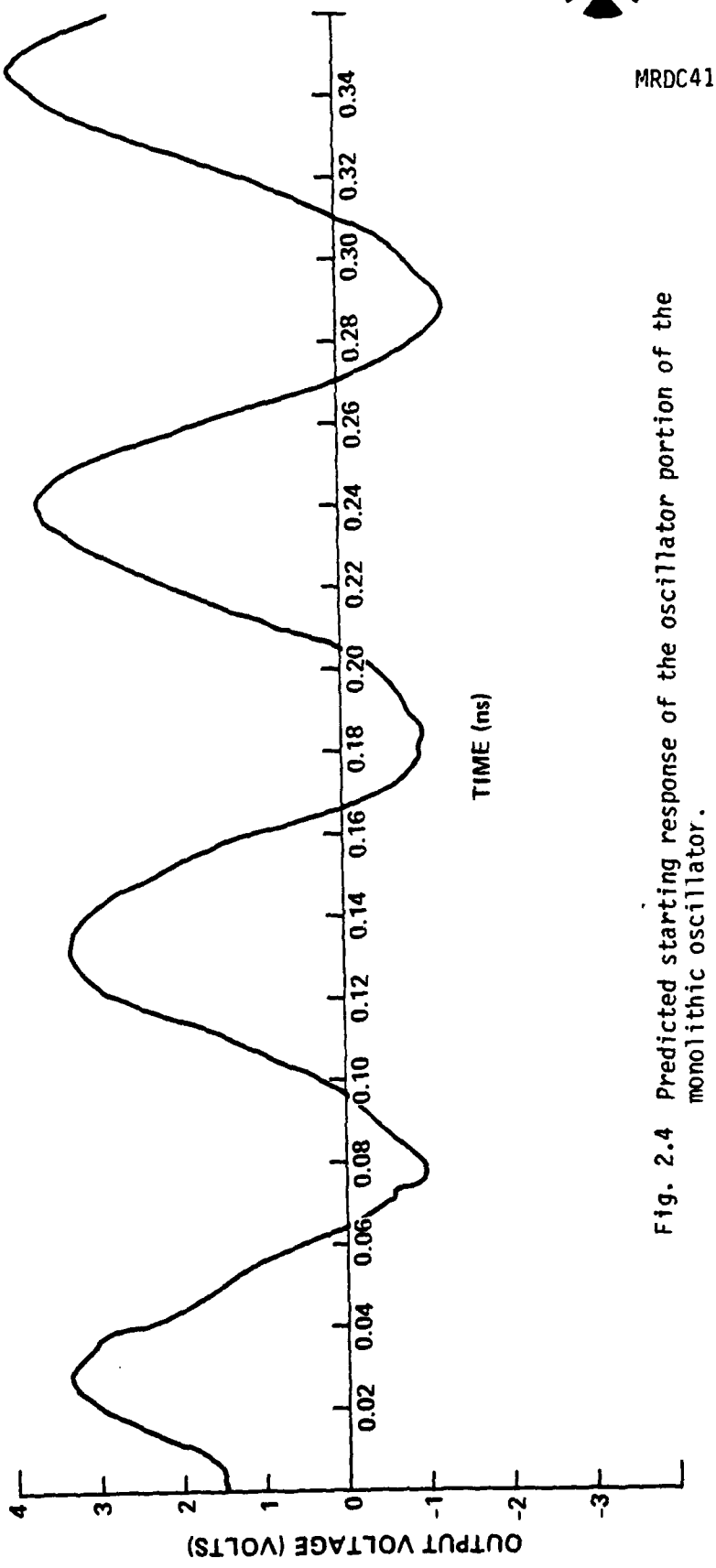

Fig. 2.4 Predicted starting response of the oscillator portion of the monolithic oscillator.

setting of the varactor tuning voltage. This simulation was not continued long enough to provide a reliable estimate of power output or harmonic content of the signal.

The predicted buffer amplifier gain and sample output gain (from the buffer amplifier input) are shown in Fig. 2.5, and the impedance match of the two outputs is shown in Fig. 2.6. These calculations are based on the detailed FET model shown in Fig. 2.7 and the layout shown in Fig. 3.6. The amplifier's reverse isolation, which is predicted to be better than 20 dB from 6 to 10 GHz, and the correct oscillator load are more important than the gain flatness. Therefore, no attempt was made to flatten the amplifier gain.

To conclude this section, Fig. 2.8 shows a typical predicted tuning curve for a common drain oscillator with G_L = 0.02, C_L = 0.4 pF, and the varactors across 3/7 of a 100 ohm shorted stub with total delay length of 7 ps. The capacitance plotted is the total capacitance of the series varactors. Figure 2.8 is based on the FET model shown in Fig. 2.7.

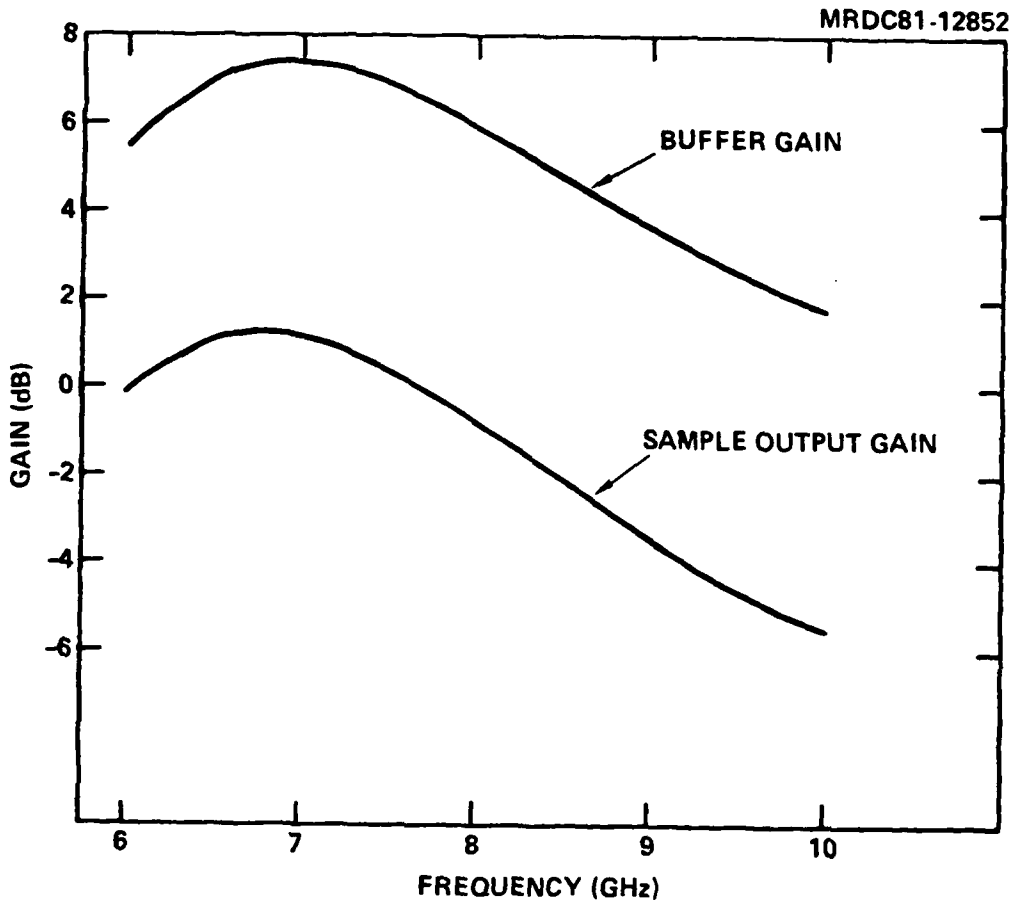

Fig. 2.5 Predicted buffer amplifier and sample output gain.

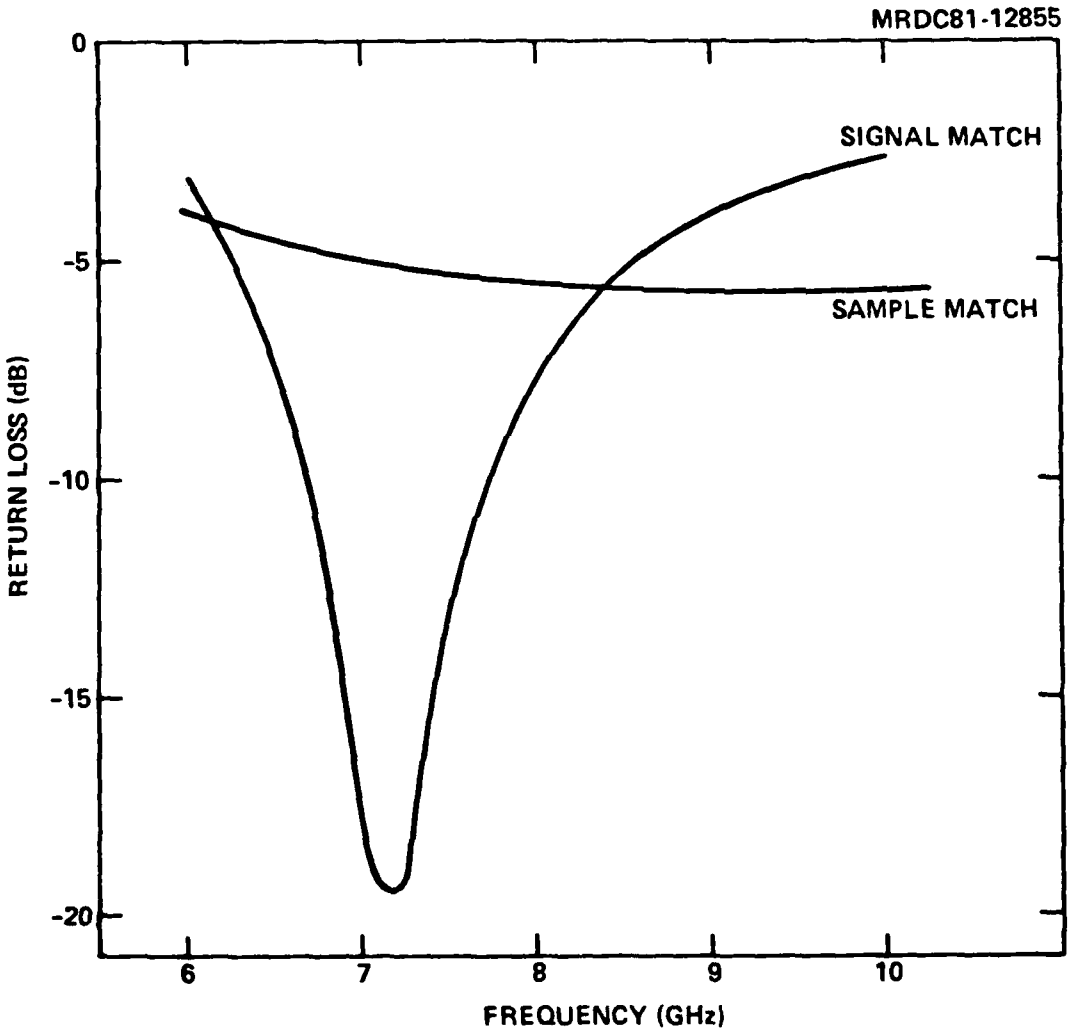

Fig. 2.6 Predicted signal and sample output matches.

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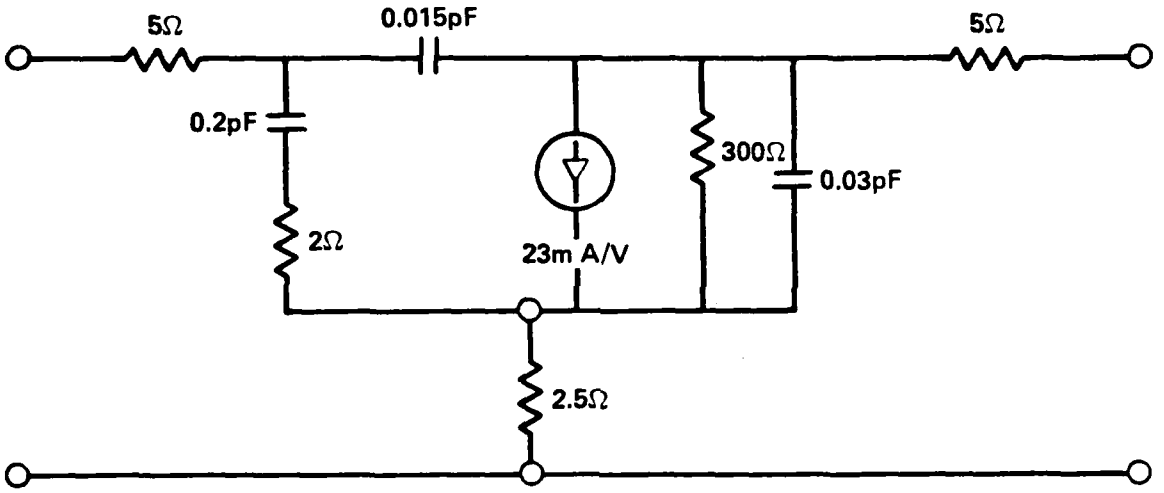

Fig. 2.7 300 μm device equivalent circuit.

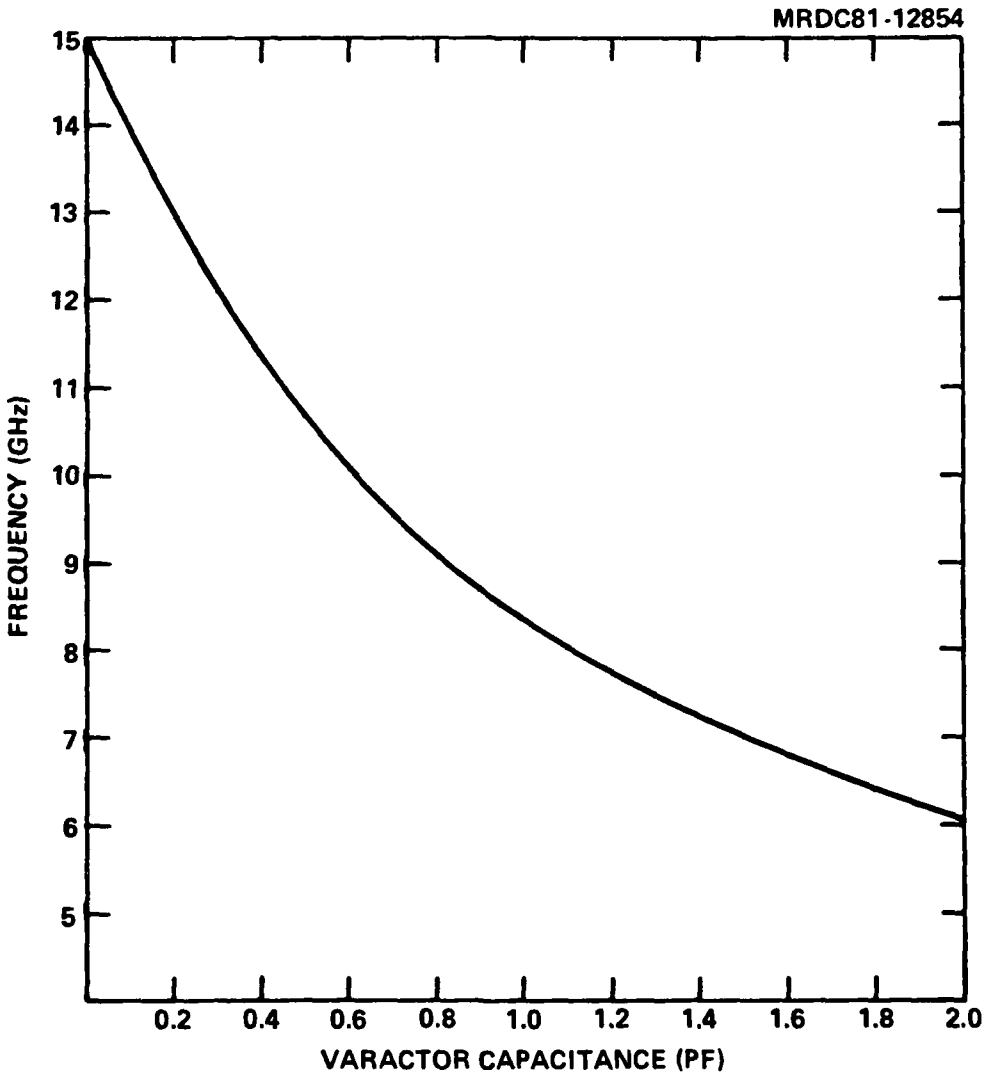

Fig. 2.8 Typical predicted oscillator tuning curve.

3.0 CIRCUIT FABRICATION TECHNOLOGY

The circuits described in this report have been fabricated on semi-insulating gallium arsenide substrates using state-of-the-art high yield processes. Complex monolithic microwave integrated circuits (MMICs) require more than one type of device (FETs, varactor diodes, etc.) for their operation and the optimization of the performance of each device may require more than one type of active layer on the same substrate. To accommodate this need, the fabrication techniques implemented in the MMIC program are based on multiple, localized ion implanted active layers leading to highly reliable planar structures. The mesa approach is also used in those cases where only one type of active layer is required. It has the advantage of increased throughput due to reduced turnaround times.

3.1 Circuit Fabrication Steps

The circuits described in this report are fabricated on 250 μm thick semi-insulating GaAs substrates using microstrip transmission line circuitry. Top surface ground planes are provided near the chip edges to allow low parasitic inductance grounding of active and passive devices.

A Si implant of 1000 Ω/□ is used for device active layers and resistors. Both interdigital and metal-insulator-metal (MIM) capacitors are used for tuning and RF bypassing purposes. Contact photolithography is used for all the steps including definition of the 1 μm gates of FETs. The mask set has six levels as described below:

Level	Function
1	Mesa/Active Layer
2	Ohmic Contact
3	Gate and First Level Metal
4	Dielectric
5	Second Level Metal
6	Fiducial Alignment Marks

The ohmic contact mask can also be used for n^+ contact implantation. However, a seventh mask level is required if the tuning varactors need a doping profile different than that of the FET active layer. Details of the important fabrication steps are given next.

1. Active layer implant: Si, Energy = 125 keV, Dose = 3.5 E12 cm^{-2} with substrate at room temperature. A peak doping of $\sim 1.5 \times 10^{17}$ cm^{-3} and a pinch-off voltage of ~3.5 volts is obtained. Definition of active areas may be accomplished by either mesa etching or by selective implantation using a photoresist mask. Fiducial alignment marks are defined on the wafer surface for subsequent realignment capability when selective implantation is used.
2. Cap and anneal: 1100Å of reactively sputtered silicon nitride is used as a cap. Annealing is done at 850°C for 30 min in hydrogen.
3. Define mesas (as necessary): This step is required only if the implantation is made over the entire wafer. Although this results in a nonplanar structure, it is often used to reduce the turnaround time. 3000Å high mesas are defined using a chemical etch ($10H_2O:1H_2O_2:1NH_4OH$).
4. Form ohmic contacts: 1000Å of eutectic composition AuGe (88% Au = 12% Ge) and 150Å Ni are evaporated using an electron beam source. Pattern definition is by the lift-off technique. The contacts are alloyed at 450°C for 1 minute in forming gas.
5. Deposit plasma silicon nitride: this nitride layer is required for reliable gate electrode definition as described below.
6. Deposit Gate and First Level Metal (Ti/Pt/Au): In order to minimize the parasitic gate resistance, the thickness of the gate metal must be made as large as practical. The yield of the gate definition step, however, decreases rapidly with increasing metal thickness for conventional photoresist lifting techniques. In order to increase the lifting capability, a

layer of silicon nitride is deposited on the GaAs and the gate pattern is defined in photoresist. The exposed nitride is then etched in a CF_4 plasma. Due to the increased distance between the top of the resist and the surface of the GaAs, thicker metallization may be deposited and lifted. Excellent edge definition is obtained by this technique. Reactive ion etching was used to etch the nitride to minimize undercutting.

The first level metallization contains the interdigital capacitors, the bottom plates of MIM capacitors, ohmic contact overlays, and interconnecting lines. In attempting to define this pattern by conventional lifting techniques, it was observed that the edges were ragged due to the tearing involved at these points. These sharp edges are not well covered by the subsequent step of dielectric deposition which forms the "I" layer of MIM capacitors. This results in a very poor yield of MIM capacitors made on wafers processed in this manner. The nitride aided lifting process eliminates the metal tearing provided that metal thickness is less than the nitride thickness. This results in smooth edges and a high yield of MIM capacitors.

7. Deposit plasma silicon nitride: This nitride layer is used as the dielectric for the MIM capacitors and as the insulator for crossovers. It also provides a protection layer for the FETs.
8. Open via holes: Via holes are opened in the silicon nitride layer wherever connections to the first level metal are desired. Standard photolithography and plasma etching is used for this purpose.
9. Deposit second level metal: This metallization (Ti/Au) is used for the top electrode of MIM capacitors and all the inter-device matching circuitry. The gold is usually electroplated to a thickness of ~2-3 μm to reduce ohmic losses.
10. Backside metallization.
11. Saw wafer into individual chips.

Figure 3.1 shows a photograph of the 2 mm × 2 mm oscillator chip. A considerable portion of the chip area is allocated to the bonding pads and bypass capacitors for easy testing and insensitivity to test fixture variations.

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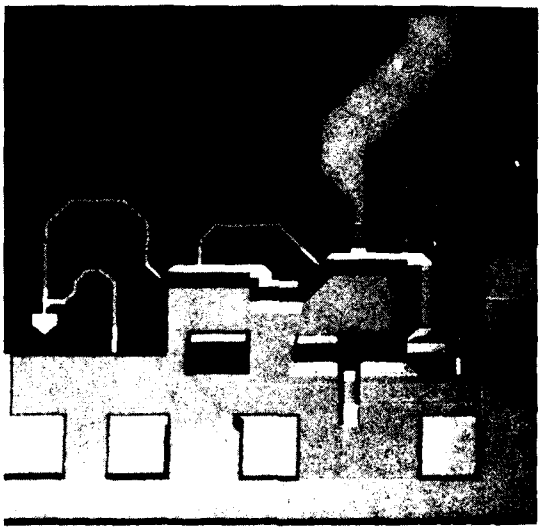

Fig. 3.1 SEM photograph of the oscillator chip.

4.0 TEST RESUTS

Measured oscillator performance data are presented in this section, followed by an analysis which leads to an improved understanding of the circuit operation and device models. Recommendations for further work to upgrade the monolithic VCO performance based on the improved models are included in Section 5.0.

4.1 Measured Performance

The free running oscillator frequency (with 0 volts across the varactor capacitance) varied from device to device but always occurred between 9.5 and 10.5 GHz. Oscillator performance is marginal as indicated by the low output power (approximately -15 dBm) and the lack of oscillation in several devices. Those devices which did not oscillate became operational when the buffer amplifier was disconnected by scribing its inductive input line. Without the buffer amplifier load impedance, the free running frequency of operation was approximately 11 GHz. Note that the 100 ohm source resistance is still present in this mode of operation. Tuning either the gate-to-source capacitance, C_{gs}, or the varactor diodes resulted in a tuning range of approximately 100 MHz. The narrow tuning range and high operating frequency indicate that the resonant circuit is not presenting an optimum impedance to the gate of the oscillator FET. Either inaccuracies in the varactor model, the FET model, or both are the likely causes of this discrepancy. The inductive transmission lines have been used in many previous designs and are modeled quite accurately, though models of stray coupling and distributed ground effects are still in need of improvement.

The gain of the buffer amplifier cannot be measured experimentally since it is an integral part of the monolithic chip. There is no input bonding pad and it is not matched to 50 ohms at the input. It is possible to measure the output match, which is shown in Fig. 4.1. The output match has a null at 7.6 GHz almost identical to the null at 7.1 GHz predicted in Fig. 2.6,

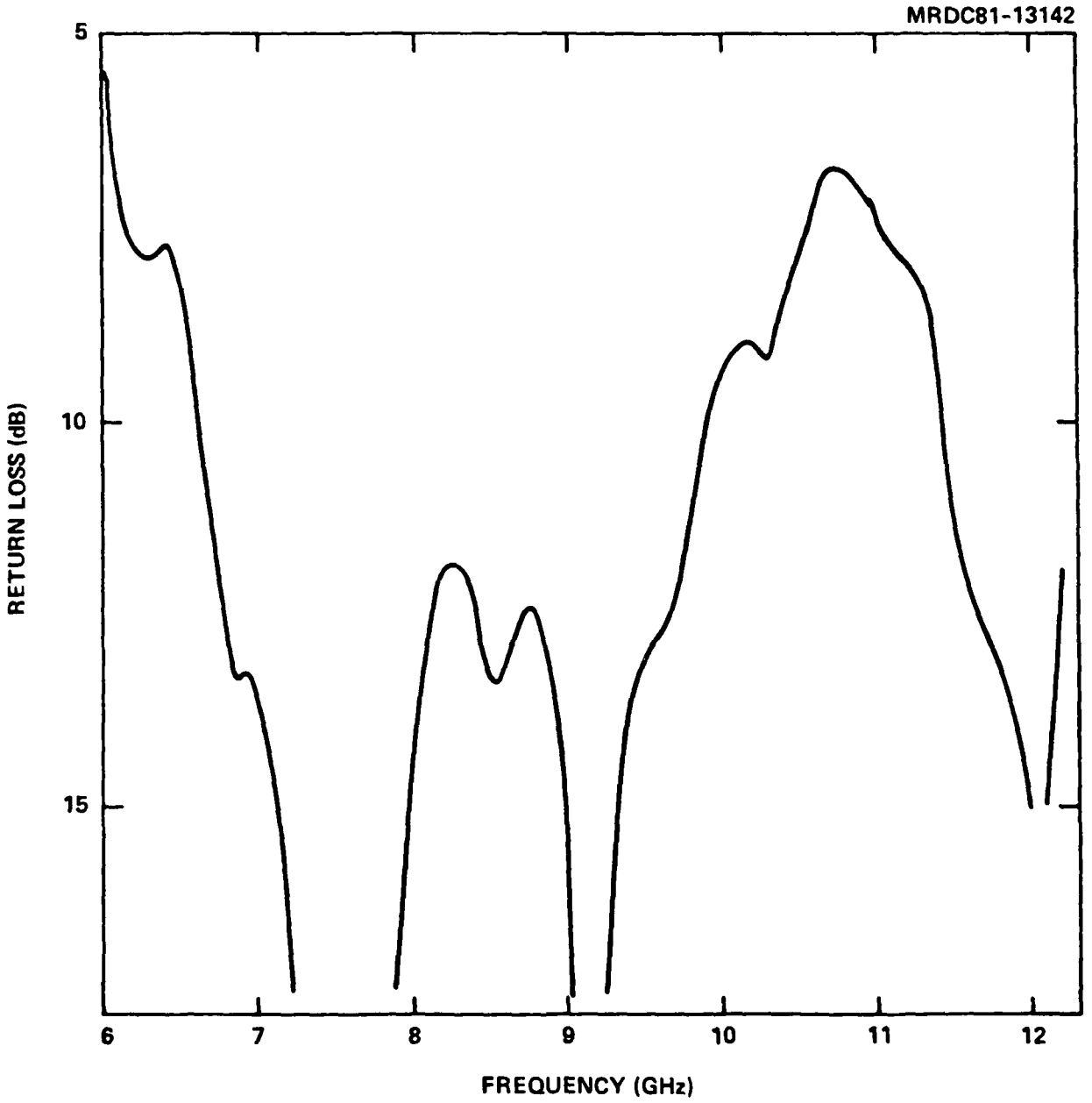

Fig. 4.1 Measured buffer amplifier output return loss.

but has extra resonances at 9.2 and 12.2 GHz. These extra resonances are likely to be lossy or radiating test fixture resonances not present in the monolithic chip. More measurements are needed to verify this hypothesis which may help to explain the low measured output power.

4.2 Performance Analysis

As indicated in the previous section, inaccurate FET or varactor models are the most likely cause for the higher than expected operating frequency. These models must be improved and an accurate model of the existing circuit must be developed to successfully design an improved oscillator for the next mask iteration. Toward this goal, the parameters in question were computer optimized to the existing performance while holding the remaining passive structures fixed. Such "reverse design" procedures are a powerful modeling tool provided care is exercised in selecting realistic variables and starting points. To further improve accuracy the oscillator without the buffer amplifier was used, thus eliminating the need to measure or model the input impedance of the buffer. Optimizing the varactor and FET parameters for a net small-signal impedance of exactly zero ohms including the 100 ohm load resistor (negative match condition) at 11 GHz, and then plotting the output admittance as a function of frequency results in the admittance plane plot shown in Fig. 4.2. Figure 4.2 also contains a plot of the negative of the predicted buffer amplifier input impedance as a function of frequency. This type of diagram interprets the resonator-FET combination as a one-port negative impedance oscillator. When plotted on the same admittance plot as the oscillator load (in this case the buffer amplifier), starting conditions of the oscillator can be evaluated. The figure predicts that the oscillator will not operate when the buffer amplifier is connected, which is indeed true in some circuits. The fact that some circuits do work (at a low output power) indicates that there is some variation from circuit to circuit, and suggests that the predicted input admittance of the buffer amplifier is not as high as estimated in Fig. 4.2.

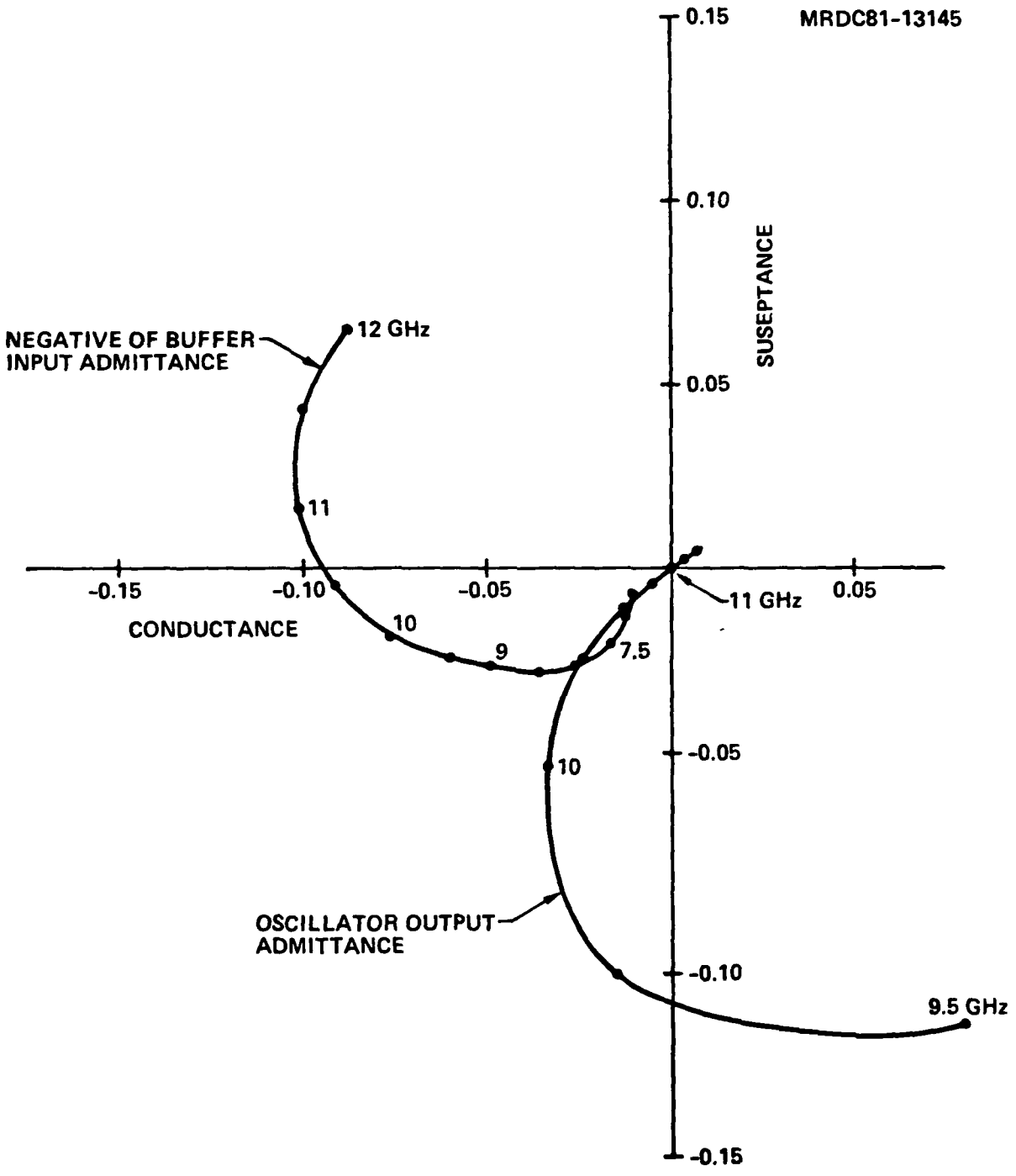

Fig. 4.2 Admittance plane plot of oscillator - buffer amplifier interface.

The above analysis leads to the conclusion that the oscillator resonant circuit should be adjusted for operation at the correct frequency, and that the buffer amplifier should be modified for improved oscillator loading and increased power output. These suggestions are described in detail in the next section.

5.0 SUMMARY AND RECOMMENDATIONS

The first phase of the monolithic stabilized oscillator program has been successfully completed, and work on the second phase is continuing as part of the 8 GHz monolithic receiver front end program, Contract No. N00014-78-C-0624. X-band oscillations available from the first generation circuits will be re-tuned to a voltage controlled frequency between 7.25 and 8.75 GHz to cover the 7.75 to 8.25 GHz satellite communications band with both a low and high side local oscillator. The oscillator will then become an integral part of the monolithic 8 GHz receiver front end chip.

To obtain acceptable performance, continuing work is required in several areas. The planar varactor diode must be upgraded, modeled more accurately, and scaled to the correct unbiased junction capacitance. In conjunction with a slight modification of the tuning inductor, proper broadband operation will then be achieved. Improved load impedance for the oscillator will increase available output power while maintaining load pull isolation. A source follower output stage should be re-considered for this application due to its small input admittance, though it will not have as much gain as the common source stage in the first generation circuit.

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